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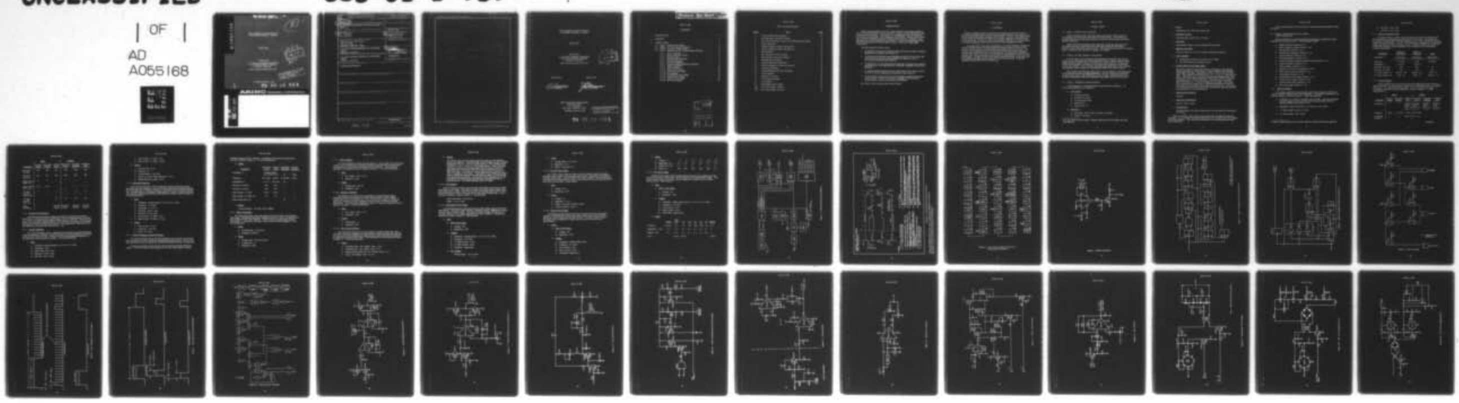

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DEVELOPMENT OF MICROCIRCUIT TELEVISION CAMERA — PHASE I

August 1969

Prepared for

U.S. NAVAL UNDERSEA RESEARCH AND DEVELOPMENT CENTER
Pasadena, California

Under Contract N66001-69-C-1200

Publication 663-01-1-989

ARINC RESEARCH CORPORATION

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Prepared by

K.J. Braman

K.J. Braman

Approved by

J.R. Gliessman

J.R. Gliessman

ARINC RESEARCH CORPORATION
Western Division
P.O. Box 1375
Santa Ana, California 92702

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LIST OF ILLUSTRATIONS

1. INTRODUCTION

Under Contract N66001-69-C-1200, ARINC Research Corporation undertook Phase I in the development of a high-sensitivity television camera utilizing thin-film microelectronic techniques. The camera is to be designed to meet the electrical performance requirements of SCD Supplement 410-290-8024, "Source Control Drawing for the Deep Submergence Rescue Vehicle (DSRV) Camera, Television, Zoom, Pan-and-Tilt;" and SCD Supplement 410-2908025, "Source Control Drawing for the Deep Submergence Rescue Vehicle (DSRV) Camera, Television, Right Angle, Topside Pan."

The tasks involved in Phase I were:

1. To establish a camera test facility having provisions for control of ambient lighting and test patterns (see Section 3);

2. To evaluate a government-owned Westinghouse Model STV/606 Secon television camera to determine the adaptability of existing circuitry to microcircuit technology (see Section 4);

3. To establish an overall implementation approach, including block diagrams, packaging plans, and requirements for monolithic integrated circuits (see Section 5);

4. To develop detailed requirements for each element in the camera system to serve as circuit design goals and guidelines (see Section 6);

5. To document the results of the overall investigation; define the proposed camera system in terms of circuitry, packaging, and performance characteristics; and include preliminary schematics.

Per Task 5, this is the final report under Phase I.

2. SUMMARY

The Westinghouse Model STV/606 Secon television camera has electrical performance characteristics compatible with the specifications for the camera to be used in the Deep Submergence Rescue Vehicle (DSRV). However, the configurations of most of the circuits in the STV/606 are not readily adaptable to thin-film microcircuit technology. The use of large-value capacitors, inductors, and transformers is the most incompatible feature of the circuits in the Westinghouse camera.

As an alternative, this study revealed that it is entirely feasible to design and build a miniature camera incorporating thin-film microcircuitry in most of the circuits, and employing a secondary electron conduction (SEC) camera tube. The circuits must be designed so as to minimize the number and value of capacitors, minimize the number of inductors and transformers, and depend where possible on resistor-value ratios rather than absolute values to permit greater control of circuit performance. An effort should also be made to maximize the use, on the thin films, of monolithic integrated circuits rather than discrete components, for greater packaging density and improved reliability.

3. PHASE I TASKS

3.1 TASK 1: CAMERA TEST FACILITY

ARINC Research set up a television-camera test facility with provision for controlling up to six 500-watt lamps from zero to full voltage. The facility also included electronic test equipment necessary to measure voltage levels and observe internal waveforms.

Light intensity measurements were taken with a Honeywell spot light meter. Horizontal and vertical resolutuions were evaluated utilizing the Electronics Industries Association (EIA) resolution chart. This chart was also used for measuring gamma, interlace, phase distortion, ringing, and linearity.

3.2 TASK 2: STV/606 CAMERA EVALUATION

The first step in the evaluation of the Westinghouse Model STV/606 camera system was to interconnect all module schematics to form a single schematic representing the entire camera system, exclusive of the power supplies. From a study of this overall schematic, the theory of operation of the system and its individual circuits was derived.* The conclusions reached during examination of the schematic were verified, where feasible, by measurements made on the camera system.

The circuits in the STV/606 camera do not, for the most part, lend themselves to thin-film microcircuit packaging techniques. The use of large-value capacitors in most of the circuits, and of inductors in many circuits, would make impractical the direct application of thin-film techniques to the design of the STV/606 camera.

3.3 TASK 3: PROPOSED CAMERA SYSTEM

A block diagram of a proposed camera system is shown in Figure 1. Its electrical specifications are as follows:

a. Scan Format

1) 525 lines per field
2) 60 fields per second
3) 30 frames per second
4) Interlaced 2:1
5) Aspect ratio, 4:3

b. Resolution

1) Horizontal: 600 TV lines, minimum, at center.
2) Vertical: 375 lines.

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*NUC was unable to obtain timely, adequate information on this subject from the manufacturer.

c. Sensor

Westinghouse WL-30691 SEC camera tube

d. Light-level control

Automatic light control (ALC): 10,000:1

e. Gray Scale

Eight shades of gray, based on standard EIA test chart.

f. Signal-to-noise ratio

37 db S/N ratio at 5 x 10^{-3} foot-candles faceplate illumination.

g. Video amplifier

1) Bandwidth plot within ±3 db from 30 Hz to 8 MHz.
2) Dc restoration by keyed clamp circuit.

h. Camera video and sync signal output

The camera video and sync signal output will conform to EIA Standard RS-330; see Figure 2, fields 1 and 2. Notes 3 through 5 and 8 through 13 of this figure will apply. Substituted for notes 1 and 2 will be the statement, "The waveform shall conform to $(\alpha + \beta)$ = 1.0 to -1.5 volts peak-to-peak." Note 6 will read: "Overshoot on horizontal blanking signal shall not exceed 0.04β at the beginning of the Front Porch and 0.1β at the end of the Back Porch." Note 7 will read: "Overshoot on the sync signal shall not exceed 0.1β." Notes 14 through 16 do not apply. This output will be present at all times (with or without the presence of an external sync signal), but the external sync signal will have priority. In the event of loss of external sync, the camera will automatically internally generate and distribute sync as described above.

i. Sweep failure protection

All axes.

j. Input power requirement

28 Vdc ± 10%; 10 watts.

k. External sync

Synchronization to be derived internally or from external sync terminated in 75 ohms.

Wherever possible, the circuits in the camera will be packaged by thin-film techniques. It is estimated that approximately 75% of the circuitry would be packaged as thin-film modules. This could be accomplished on an estimated eight one-inch-square substrates.

A flow chart depicting a typical process for producing a hybrid module is shown in Figure 3.

3.4 TASK 4: REQUIREMENTS FOR CAMERA SYSTEM ELEMENTS

Given in this section are specifications and preliminary schematics of major elements of the camera circuitry. These elements include:

a. Master oscillator (Section 3.4.1)

b. Binary frequency divider (Section 3.4.2)

c. Sync generator (Section 3.4.3)

d. Alternate sync generator* (Section 3.4.4)

e. Vertical deflector (Section 3.4.5)

f. Horizontal deflector (Section 3.4.6)

g. Camera blanking and sweep-protection circuit (Section 3.4.7)

h. Video preamplifier (Section 3.4.8)

i. Video amplifier (Section 3.4.9)

j. Aperture correction circuit (Section 3.4.10)

k. Video clamp and mixer (Section 3.4.11)

l. ALC detector (Section 3.4.12)

m. Photocathoder power supply (Section 3.4.13)

n. Primary power supply (Section 3.4.14)

o. Camera power supply (Section 3.4.15)

p. SEC power supply (Section 3.4.16).

3.4.1 Master Oscillator

The crystal-controlled master oscillator generates a frequency stable pulse train for internal timing and sync signal generation. A preliminary schematic of the master oscillator is shown in Figure 4. Output specifications:

a. Frequency: 31.5 kHz or 2.016 MHz, both ±0.005%. (The choice between the two frequencies will be based on the option selected for the sync generator design; see Section 3.4.3.)

b. Amplitude: Square wave from 0 ± 0.1 volts to 5 ± 0.3 volts.

c. "1" state current: source, 0.12 mA

d. "0" state current: sink, 10 mA

---

*If used, would substitute for the binary frequency divider and the sync generator.

e. Rise time: 80 ns, max.

f. Fall time: 30 ns, max.

3.4.2 Binary Frequency Divider

The binary frequency divider receives inputs from the master oscillator and provides outputs for timing the horizontal and vertical circuits. The divider has two outputs, one being half of the input frequency, or 15.25 kHz; and the second being 1/525 of the input frequency, or 60 Hz. The preliminary schematics of two alternative design approaches are shown in Figures 5 and 6. Further evaluation is needed concerning the advantages and disadvantages of each alternative in this application. Circuit specifications:

Parameter	Output #1 (Horizontal)	Output #2 (Vertical)	Input
Amplitude, V	Pulse train, 0 ± 0.1 to 5 ± 0.3	Pulse train, 0 ± 0.1 to 5 ± 0.3	Square wave, 0 ± 0.1 to 5 ± 0.3
Frequency	15.75 kHz	60 Hz	31.5 kHz
Pulsewidth, us	2 to 20	2 to 100	-
Rise time, ns (max)	500	500	80
Fall time, ns (max)	100	100	30
"1" state current, uA	Source: 120	Source: 120	Sink: 20
"0" state current, mA	Sink: 12	Sink: 12	Source: 1.5

3.4.3 Sync Generator

When provided with the vertical and horizontal trigger inputs from the binary frequency divider, the sync generator produces 1) vertical drive pulses, 2) horizontal drive pulses, 3) a composite blanking signal, and 4) a composite sync signal. A preliminary schematic of the sync generator is shown in Figure 7. Circuit specifications:

	Inputs			Outputs		
Parameter	Vertical Trigger	Horizontal Trigger	Vertical Drive	Horizontal Drive	Composite Blanking	Composite Sink
Amplitude, V	5	5	Positive pulse, 0 ± 0.1 to 5 ± 0.3	Positive pulse, 0 ± 0.1 to 5 ± 0.3	Positive pulse, 0 ± 0.1 to 5 ± 0.3	Positive pulse, 0 ± 0.1 to 5 ± 0.3
Frequency	60 Hz	15.75 kHz	60 Hz	15.75 kHz	-	-
Pulsewidth, us (min)	2	2	500 ± 50	4 ± 0.5	-	-

(continued)

Parameter	Inputs		Outputs			
	Vertical Trigger	Horizontal Trigger	Vertical Drive	Horizontal Drive	Composite Blanking	Composite Sink
Rise time, ns (max)	500	500	500	500	500	500
Fall time, ns (max)	100	100	500	500	500	500
Input current (false), mA	3	3	-	-	-	-
Input current (true), mA	0.04	0.04	-	-	-	-
"1" state current - source, mA	-	-	5	5	5	5
"0" state current - sink, mA	-	-	40	40	40	40
Delay, Waveform	-	-	See Fig. 8 and 9	See Fig. 8 and 9	See Fig. 8 and 9	See Fig. 8 and 9

3.4.4 Alternate Sync Generator

The alternate sync generator (Figure 10) performs the functions of both the binary frequency divider and the sync generator, and is a design alternative for these two circuits. Its input from the master oscillator will be 2.016 MHz. This allows all pulses to be generated by digital methods, which eliminates the necessity of providing adjustments for the various pulses and delays. The output would be the same as the sync generator previously described (Section 3.4.3).

3.4.5 Vertical Deflection

The vertical deflection circuit, triggered by the vertical drive pulses generated in the sync generator, generates a linear sawtooth current to be applied to the vertical deflection coils of the SEC tube. Figures 11 and 12 are preliminary schematics of two alternative vertical-deflection circuits. Circuit specifications:

a. Input

1) Amplitude: positive pulses, 0 ± 0.1 to 5 ± 0.3 volts
2) Frequency: 60 Hz
3) Pulse width: 500 ± 50 us
4) Rise time: 500 ns, max.
5) Fall time: 500 ns, max.

6) Input current, "1" state: 1 mA

7) Input current, "0" state: 0.2 mA

b. Output

1) Peak current: 35 mA

2) Linearity: 2%

3) Load resistance: 200 ohms

4) Output dc current range (centering): ±4 mA

5) Height adjustment range: 10 mA

3.4.6 Horizontal Deflection

The horizontal deflection circuit, triggered by the horizontal drive signal developed in the sync generator, provides a series of generally rectangular pulses. Due to the high ratio of inductive reactance to resistance in the horizontal deflection coil, the application of a rectangular voltage pulse will result in a sawtooth current. The proposed configuration of the horizontal deflection circuit is shown in Figure 13. Circuit specifications:

a. Input

1) Amplitude: Positive pulse, 0 ± 0.1 to 5 ± 0.3 volts

2) Frequency: 15.75 kHz

3) Pulsewidth: 4 ± 0.5 us

4) Rise time: 500 ns, max.

5) Fall time: 500 ns, max.

6) Input current, "1" state: 1 mA

7) Input current, "0" state: 0.2 mA

b. Output

1) Peak current: 170 mA

2) Frequency: 15.75 kHz

3) Load: 4 Ω, 1 mH

3.4.7 Camera Blanking and Sweep Protection

The camera blanking circuit provides blanking pulses (horizontal and vertical) that are applied to the SEC cathode for blanking during sweep retrace. Inputs to the blanking circuit are the horizontal and vertical drive outputs from the sync generator.

The sweep protection circuit monitors the horizontal and vertical deflection signals. In the event either of these signals is lost, the circuit applies a positive

blanking voltage to the SEC cathode. A preliminary schematic for these circuit functions is shown in Figure 14. Circuit specifications:

a. Inputs

Parameter	Horizontal Drive	Vertical Drive	Horizontal Deflection	Vertical Deflection
Amplitude, V	Positive pulses, 0 ± 0.1 to 5 ± 0.3		40	8 (pk)
Frequency	15.75 kHz	60 Hz	15.75 kHz	60 Hz
Pulsewidth, us	5 ± 0.5	500 ± 50	60	-
Rise time, ns (max)	500	500	-	-
Fall time, ns (max)	500	500	-	-
Input current, "1" state	20 nA	20 uA	-	-
Input current, "0" state, mA	1.5	1.5	-	-
Input current peak, mA	-	-	10	6

b. Outputs

Camera blanking: +30 volts to SEC cathode.

3.4.8 Video Preamplifier

The video preamplifier couples the signal from the SEC tube to the following video stages, matching the high output impedance of the SEC tube to the relatively low input impedance of the video amplifier. The circuit has no voltage gain and high current gain. A preliminary schematic of this circuit is shown in Figure 15. Circuit specifications:

a. Inputs

1) Current range: 2 to 300 nA
2) Impedance: 500 KΩ

b. Output

1) Voltage range: 200 uV to 30 mV
2) Voltage gain: ~1
3) Impedance: 250Ω

3.4.9 Video Amplifier

The video amplifier 1) boosts the video signal to a level usable in the video mixer circuit; and 2) compensates for undesired frequency and phase shift characteristics introduced by the camera tube and preamp input capacitances. The preliminary schematic of the proposed circuit is shown in Figure 15. Circuit specifications:

a. Input

1) See "Output," Sect. 3.4.8.

2) Impedance: 50Ω

b. Output

1) Voltage gain: 50 to 60

2) Impedance: 50Ω

3.4.10 Aperture Correction

The aperture correction circuit compensates for high-frequency signal attenuation caused by the inability of the SEC electron beam to resolve details smaller than its cross-sectional area. The circuit must be capable of making the necessary corrections in signal magnitude versus frequency without introducing phase shifts. The preliminary schematic in Figure 16 contains a proposed circuit for aperture correction. Circuit specifications:

a. Input

1) See "Output," Sect. 3.4.9.

2) Impedance: 25Ω

b. Output

1) Voltage gain: ~1

2) Impedance: 25Ω

3.4.11 Video Clamp and Mixer

The video clamp and mixer 1) restores the dc component of the video signal loss due to capacitive coupling in the video amplifier, and 2) combines the video signal with the composite blanking and composite sync outputs from the sync generator to produce the composite video output. The preliminary circuit schematic is shown in Figure 17. Circuit specifications:

a. Inputs

1) Composite video: See "Output," Sect. 3.3-h.

2) Composite sync: See "Output," Sect. 3.4.3.

3) Shading and horizontal tilt: See "Output," Sect. 3.4.6.

4) Video: See "Output," Sect. 3.4.10.

b. Outputs

The camera video and sync signal output will conform to EIA Standard RS-330 (see Figure 2). Notes 3 through 5 and 8 through 13 apply as stated. Substituted for notes 1 and 2 will be the statement, "The waveform shall conform to $(\alpha + \beta) = -1.0$ to -1.5 volts peak-to-peak." Note 6 will read: "Overshoot on horizontal blanking signal shall not exceed 0.04β at the beginning of the Front Porch, and 0.1β at the end of the Back Porch." Note 7 will read: "Overshoot on the sync signal shall not exceed 0.1β." Notes 14 through 16 do not apply. This output will be present at all times (with or without the presence of an external sync signal), but the external sync signal will have priority. In the event of loss of external sync, the camera will automatically generate internally and distribute sync as described above. The output impedance will be 75 ohms.

3.4.12 ALC Detector

The ALC detector monitors the level of the video signal and produces a signal proportional in dc voltage. The output dc voltage controls the output voltage of the photocathode power supply, thereby increasing or decreasing the gain of the camera tube and allowing the camera to operate over a wide range of light levels. A preliminary schematic is shown in Figure 18. Specifications:

Input video signal: 10 to 150 mV

Output: 1 to 3.5 volts.

3.4.13 Photocathode Power Supply

The photocathode power supply generates the high voltage required by the SEC photocathode. This power supply contains a switching inverter triggered by a signal from the camera timing circuits. The output voltage is voltage controlled over a specified range by an ALC signal generated in the video amplifier. A preliminary schematic is shown in Figure 19. Specifications:

a. Input

1) DSRV Power Supply

a) Voltage: 28V

b) Regulation: ±10%

2) Trigger

a) Amplitude: Positive pulse, 0 ± 0.1 to 5 ± 0.3 volts

b) Frequency: 15.75 kHz

c) "1" state current: 1 mA

d) "0" state current: 20 uA

e) Waveform: square wave

3) ALC Voltage

Voltage range: 1 to 3.5 volts

b. Output

1) Voltage range: 2.5 to 8 kV
2) Regulation: ±1%
3) Ripple: Less than 0.1%

3.4.14 Primary Power Supply

The primary power supply provides a positive voltage to power the master oscillator, binary counter, and sync generator circuits. Input power is supplied by the DSRV power supply. The remainder of the power supplies in the camera utilize switching inverters stimulated by a pulse train obtained from the circuits powered by the primary power supply. Specifications:

a. Input

1) Voltage: 28V
2) Regulation: ±10%

b. Output

1) Voltage: 5V
2) Regulation: ±0.1%
3) Ripple: Less than 1% peak-to-peak
4) Current capacity: 500 mA

3.4.15 Camera Power Supply

The deflection power supply provides the necessary positive and negative voltages not available from the primary power supply to power the horizontal deflection, vertical deflection, and video circuits. The power supply contains a switching inverter triggered by a signal from the camera timing circuits. Specifications:

a. Inputs

1) DSRV Power Supply

a) Voltage: 28V
b) Regulation: ±10%

2) Trigger

a) Amplitude: Positive square wave
b) Frequency: 15.75 kHz
c) True current: 1 mA
d) False current: 20 uA
e) Pulsewidth: Square wave

b. Output

		+6	-6	+15	-15	+20	+30
1)	Voltage, V	+6	-6	+15	-15	+20	+30
2)	Regulation, Pct.	0.1	0.1	0.1	0.1	0.1	0.1
3)	Ripple (P-P), Pct.	1	1	1	1	1	1
4)	Load, mA	300	400	100	200	150	50

3.4.16 SEC Power Supply

The SEC power supply (Figure 20) generates the power levels necessary for the operation of the SEC camera tube, with the exception of the photocathode voltage. This power supply contains a switching inverter triggered by a signal from the camera timing circuits. Specifications:

a. Input

1) DSRV Power Supply

a) Voltage: 28V

b) Regulation: ±10%

2) Trigger

a) Amplitude: Positive square wave, 0 ± 0.1 to 5 ± 0.3 volts

b) Frequency: 15.75 kHz

c) True current: 1 mA

d) False current: 20 uA

e) Pulse width: Square wave

b. Output

	Target	Align Coil	G1	G2	G3	G4	G5	Heater
Voltage, V	10 to 30	18	20	-40	+300	+360	+15	6.3
Regulation, ± Pct.	0.1	0.1	0.1	0.1	0.1	0.1	0.1	1
Ripple, ± Pct.	0.1	0.1	0.1	0.1	0.1	0.1	0.1	1
Load		40 mA	50 mA					1 watt

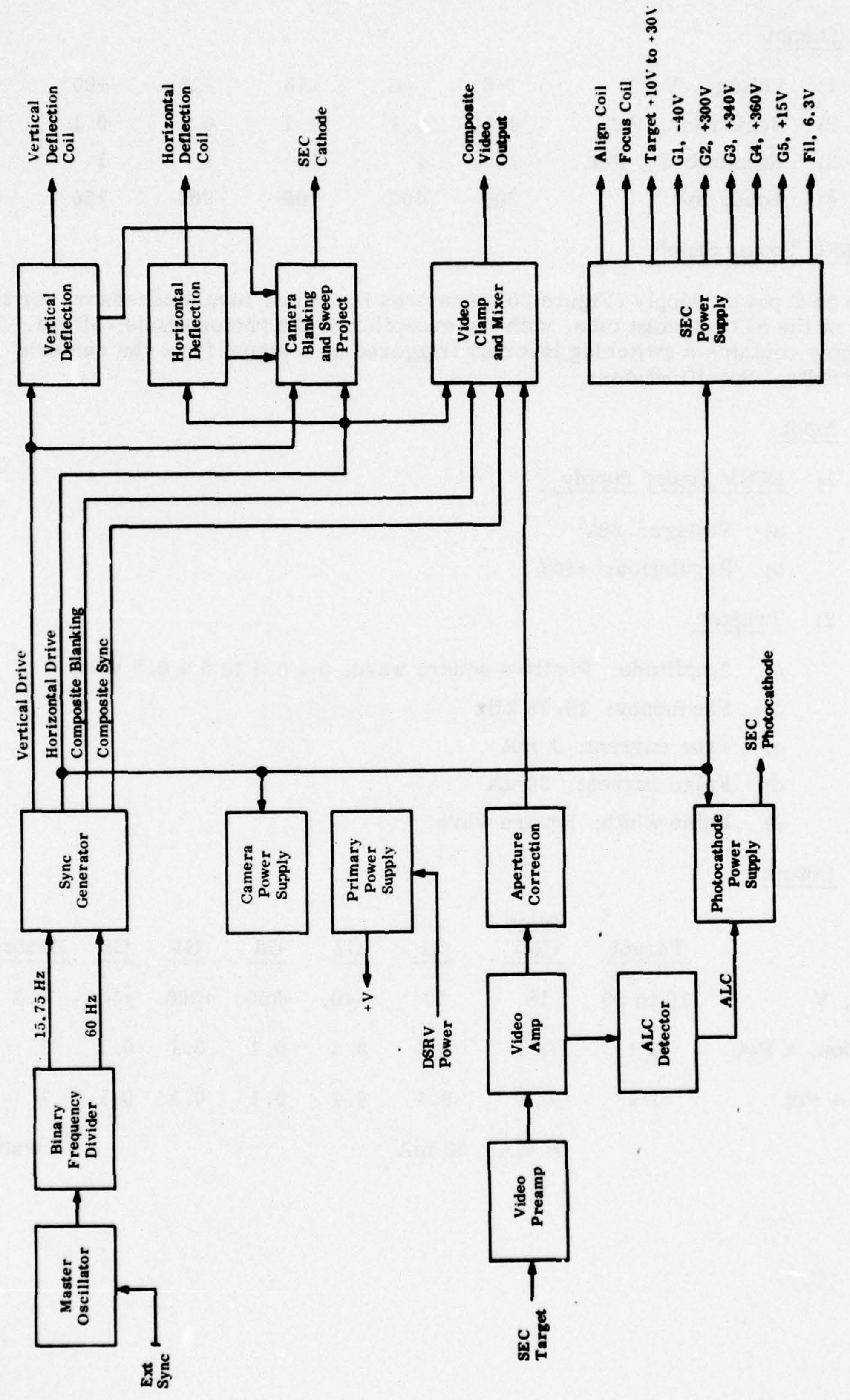
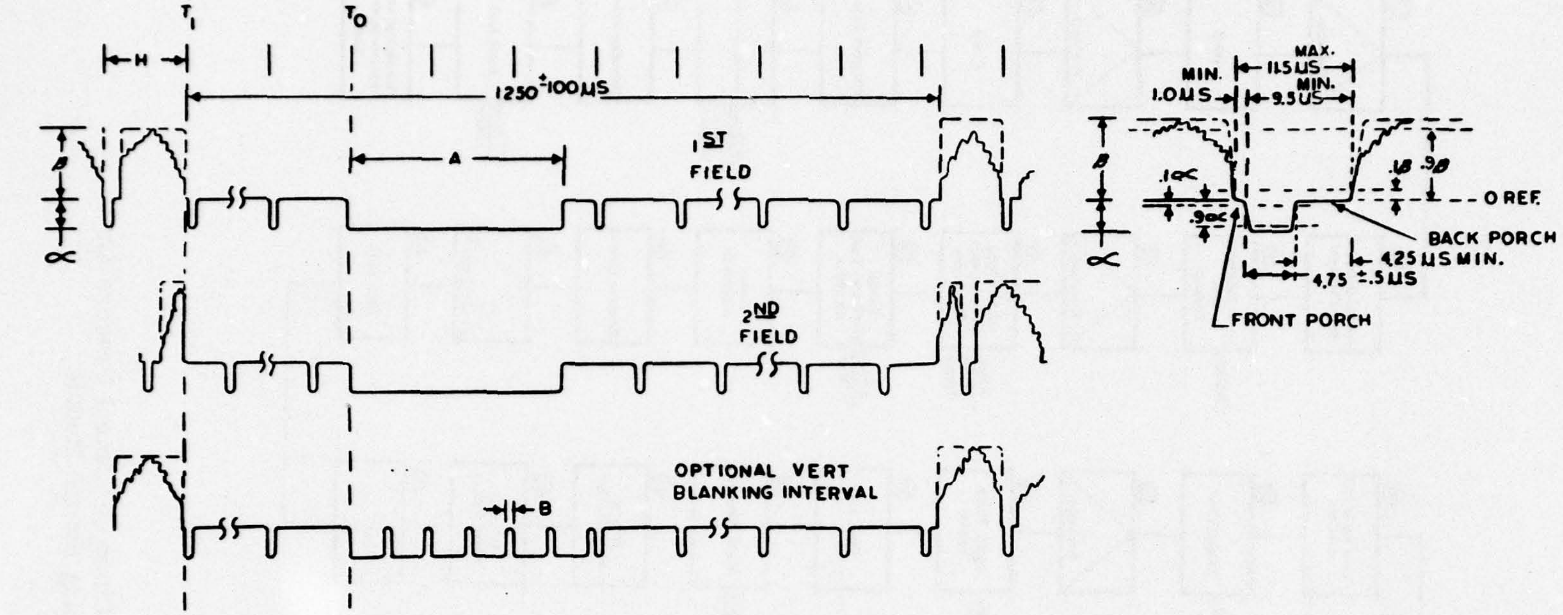


Figure 1. Camera System Block Diagram

COMPOSITE VIDEO WAVEFORM
525/60 INTERLACED 2:1



NOTES:

1. $\beta = 0.714 \pm .1$ volts (100 IRE Units).
2. $\propto = 0.286$ (40 IRE Units) nominal.
3. Sync to total signal ratio $\left(\frac{\propto}{\beta + \propto}\right) \doteq (28.6 \pm 5)\%$.
4. Blanking $= 7.5 \pm 5$ IRE Units (2.5% to 12.5% of β).
5. Horizontal Rise times measured from 10% to 90% amplitudes shall be less than 0.3μ/s.
6. Overshoot on horizontal blanking signal shall not exceed 0.02β at beginning of front porch and 0.05β at end of back porch.
7. Overshoot on sync signal shall not exceed 0.05β.
8. T_0 = start of vertical sync pulse.
9. T_1 = start of vertical blanking.
10. $T_1 = T_0 \begin{smallmatrix} +0 \\ -250\mu/s \end{smallmatrix}$.
11. A – vertical sync pulse $= 150 \pm 50\mu$/s measured between 90% amplitude points.
12. Rise and fall times of vertical blanking and vertical sync pulse, measured from 10% to 90% amplitudes, shall be less than 5μ/s.
13. Tilt on vertical sync pulse shall be less than $0.1\propto$
14. If horizontal information is provided during the vertical sync pulse it must be at 2H rate and as shown in the optional vertical blanking interval waveform.
15. B – vertical serration $= 4.5 \pm .5\mu$/s measured between the 90% amplitude points. Rise times measured from 10% to 90% amplitudes shall be less than 0.3μ/s.
16. If equalizing pulses are used in the vertical blanking interval waveform they shall be 6 in number preceding the vertical sync pulse and be at 2H rate.

Figure 2. Recommended Composite Waveform

From EIA Standard RS-330, Nov. 1966, "Electrical Performance Standards for Closed Circuit Television Camera 525/60 Interlaced 2:1."
Reprinted courtesy of Electronics Industries Association.

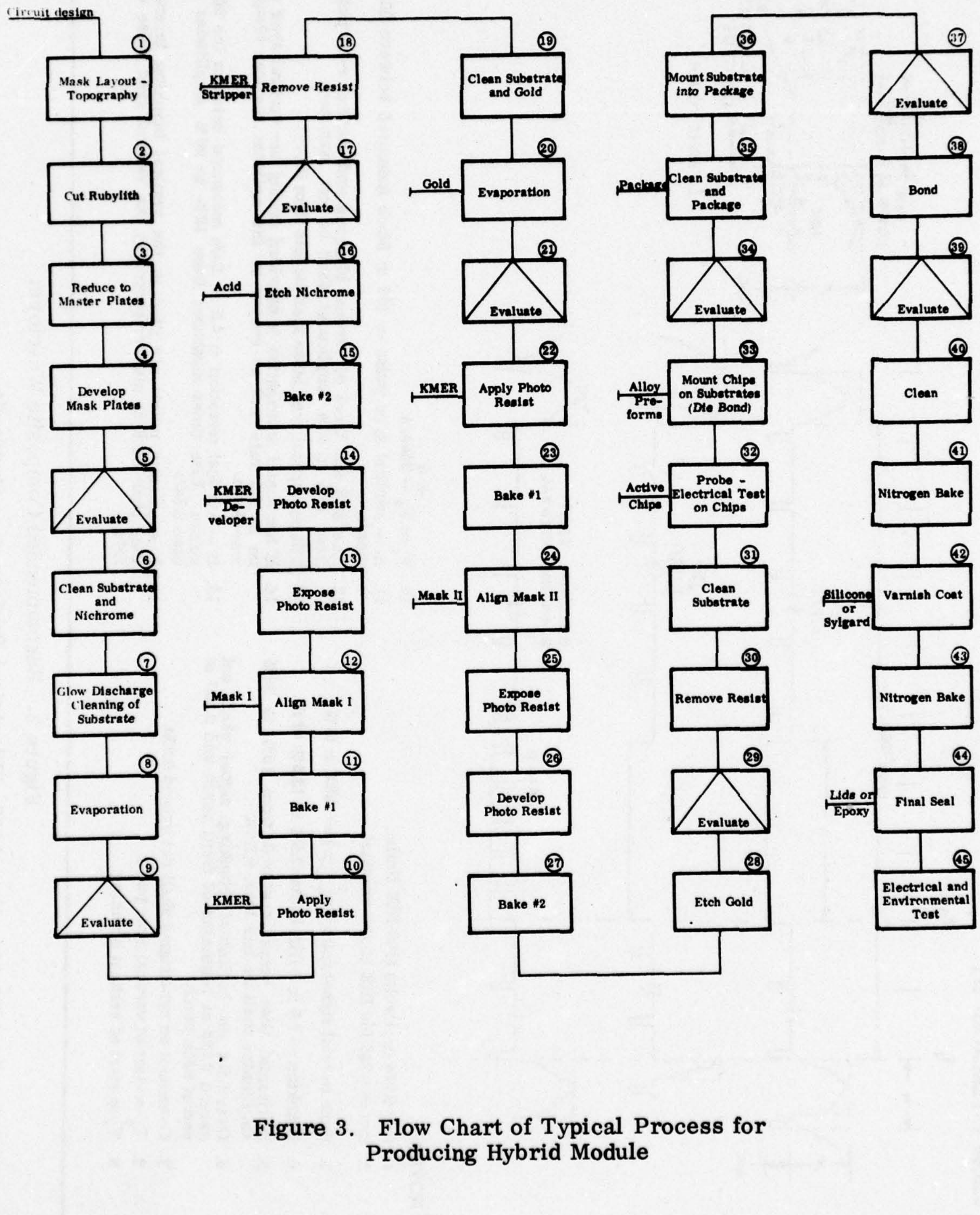


Figure 3. Flow Chart of Typical Process for Producing Hybrid Module

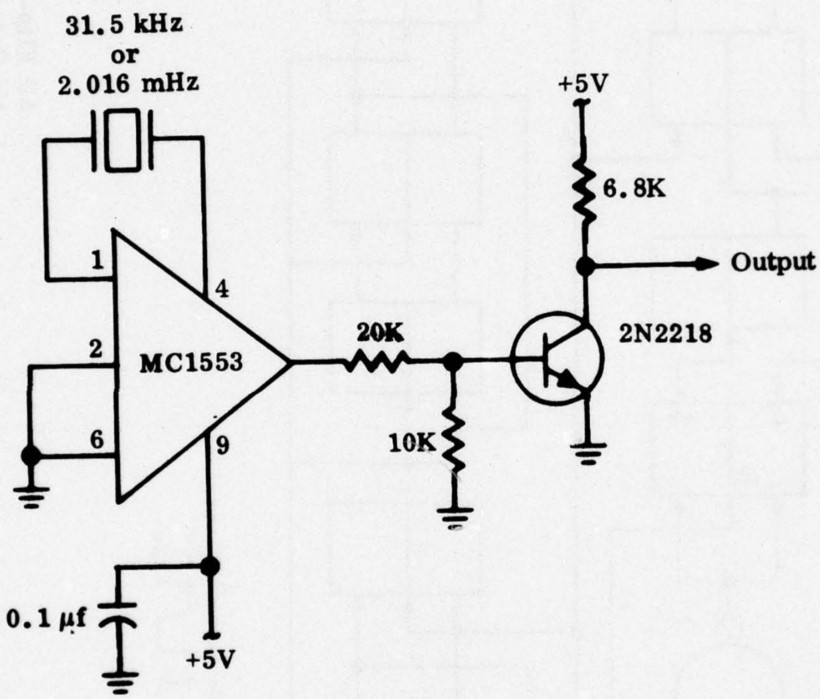
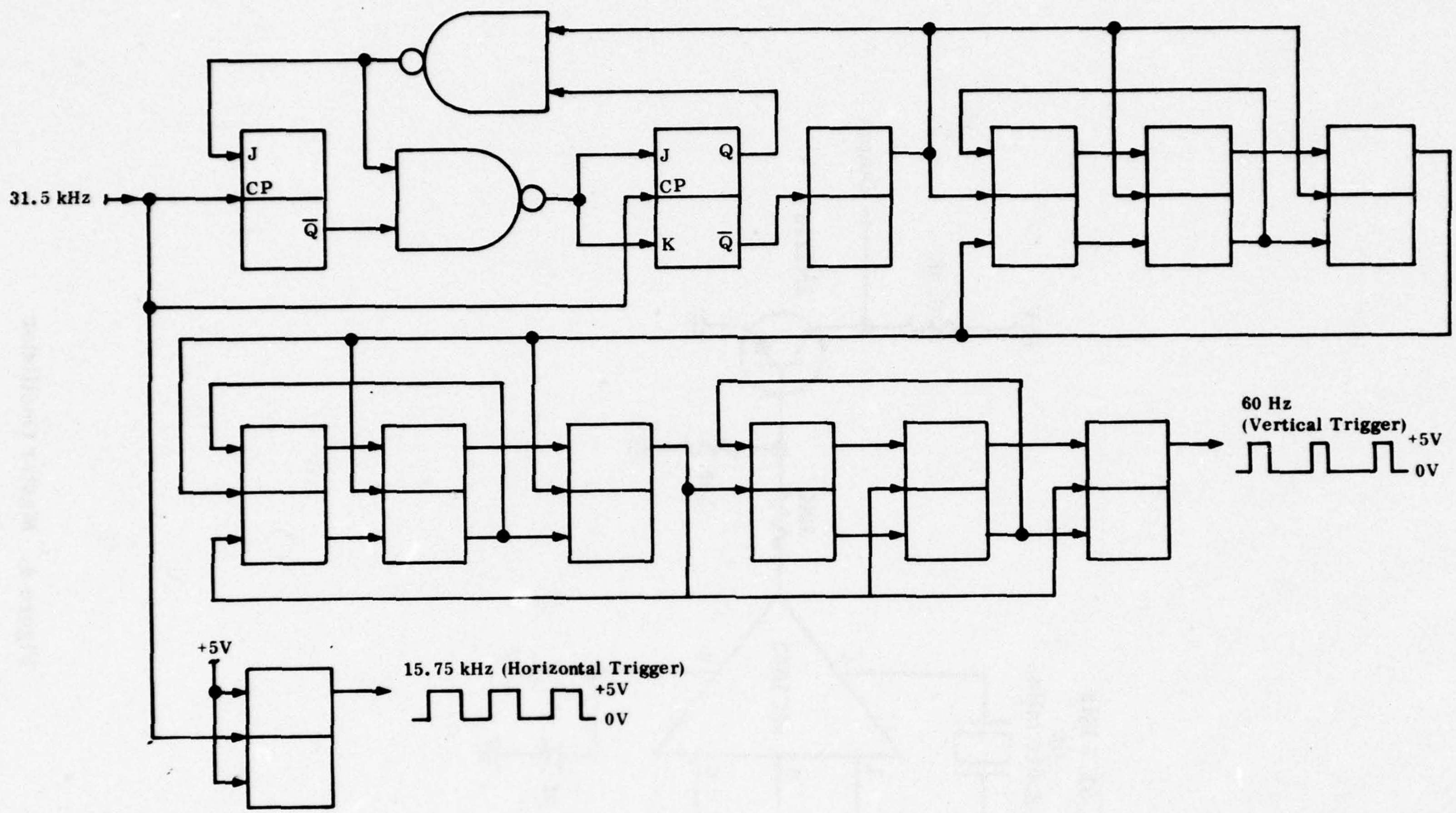


Figure 4. Master Oscillator



All Flip-Flops are Motorola MC853
All Gates are Motorola MC846

Figure 5. Binary Frequency Divider (Alternate #1)

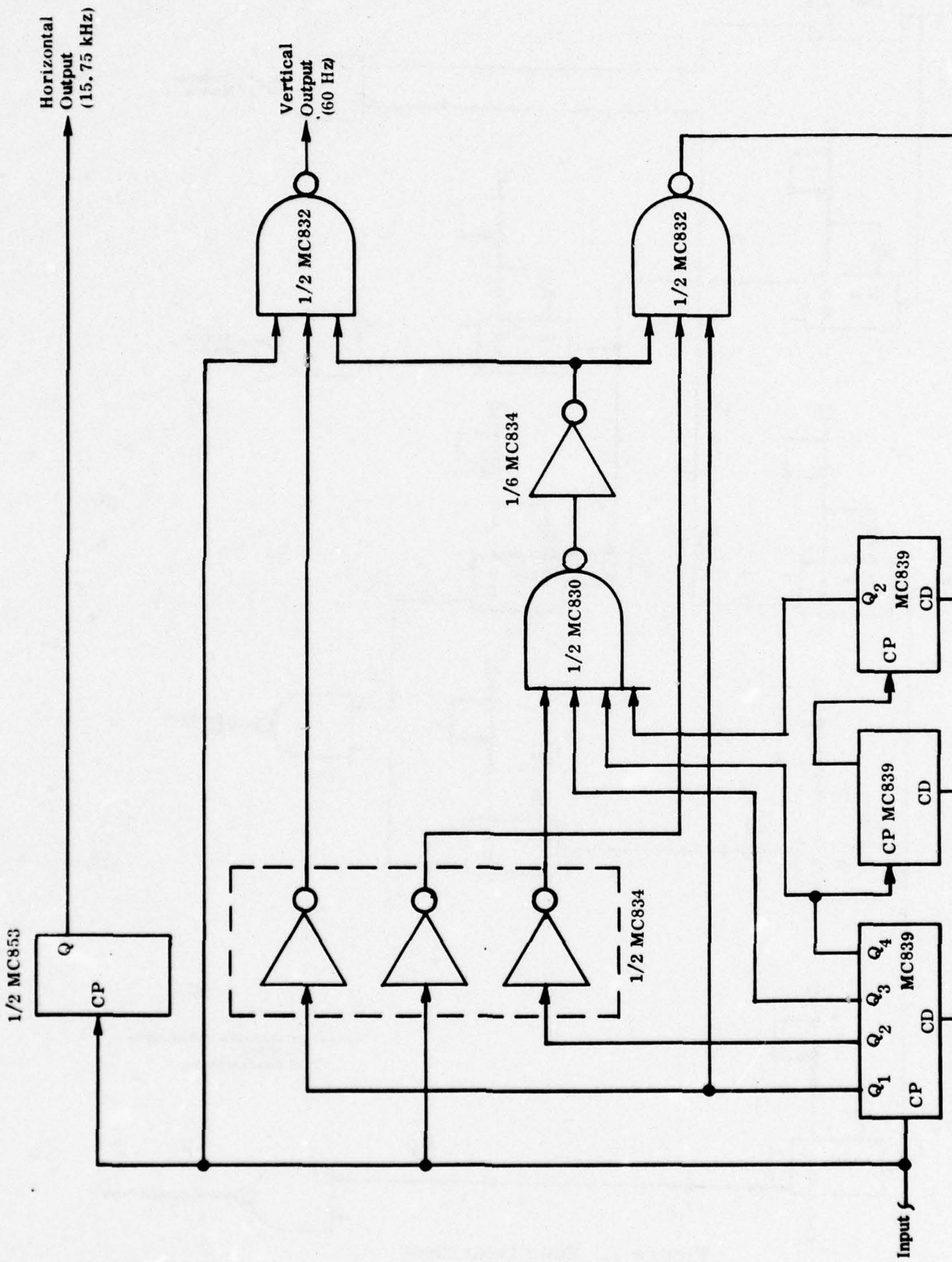


Figure 6. Binary Frequency Divider (Alternate #2)

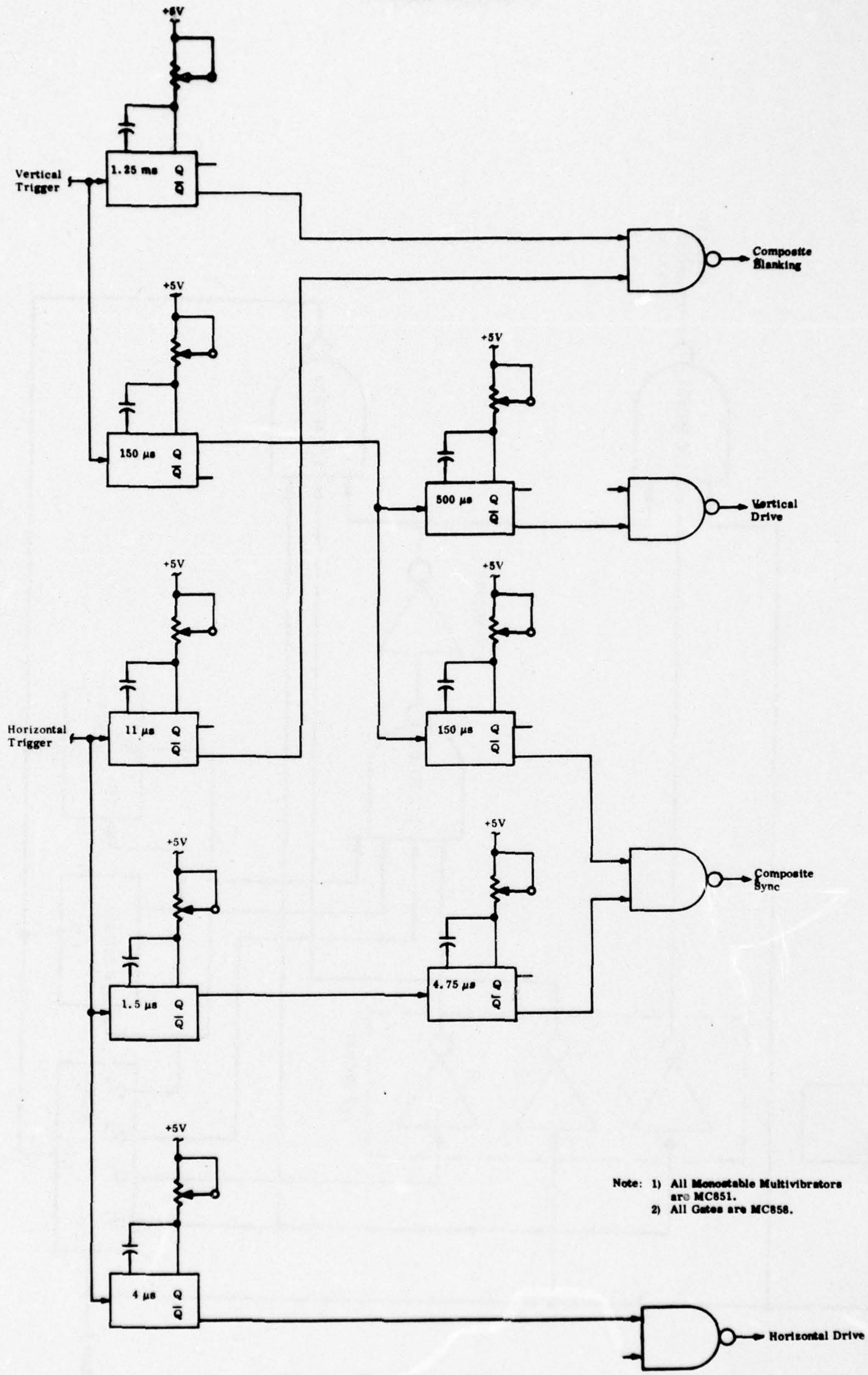


Figure 7. Sync Generator

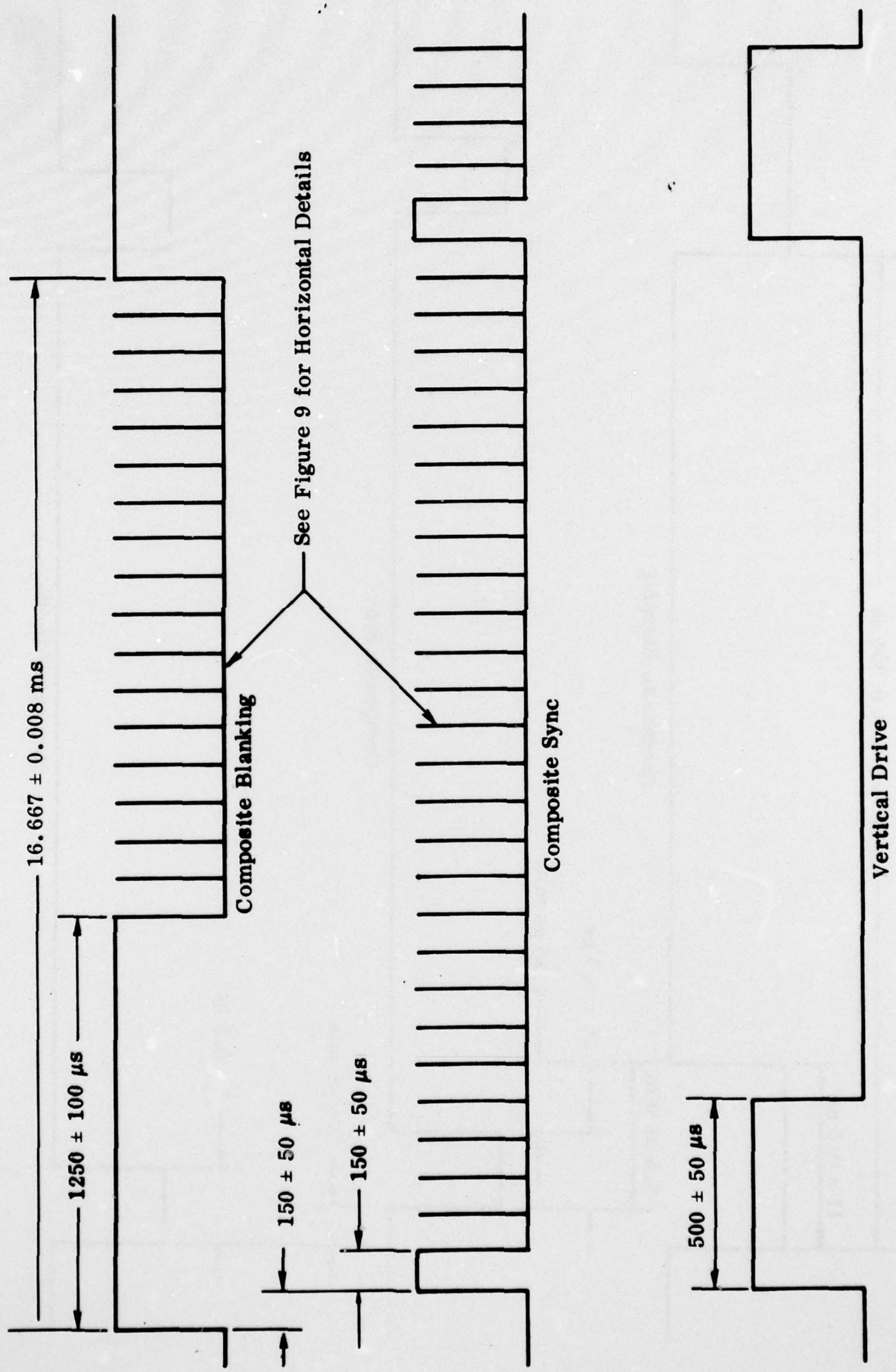


Figure 8. Sync Generator Vertical Outputs

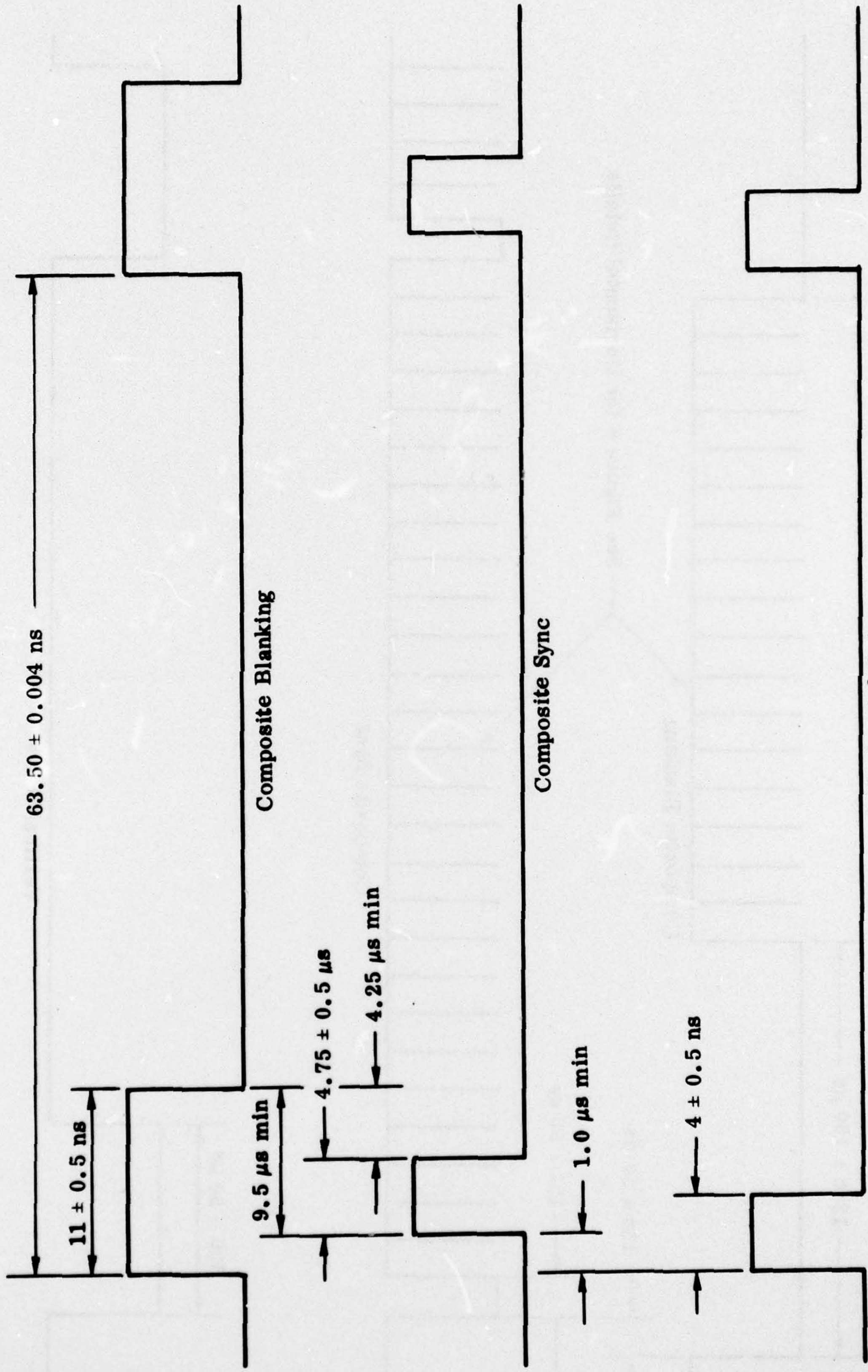


Figure 9. Sync Generator Horizontal Outputs

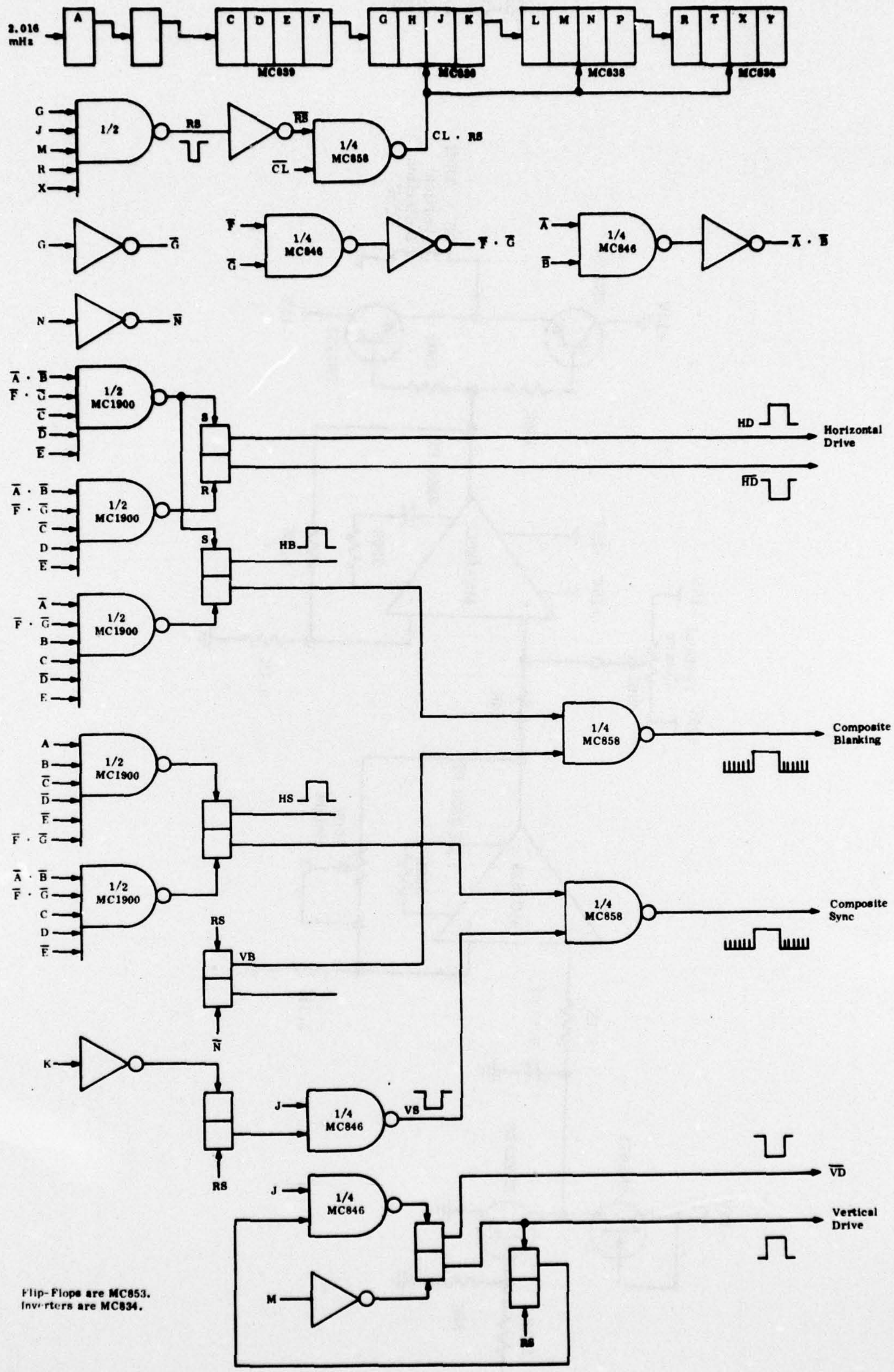


Figure 10. Alternate Sync Generator

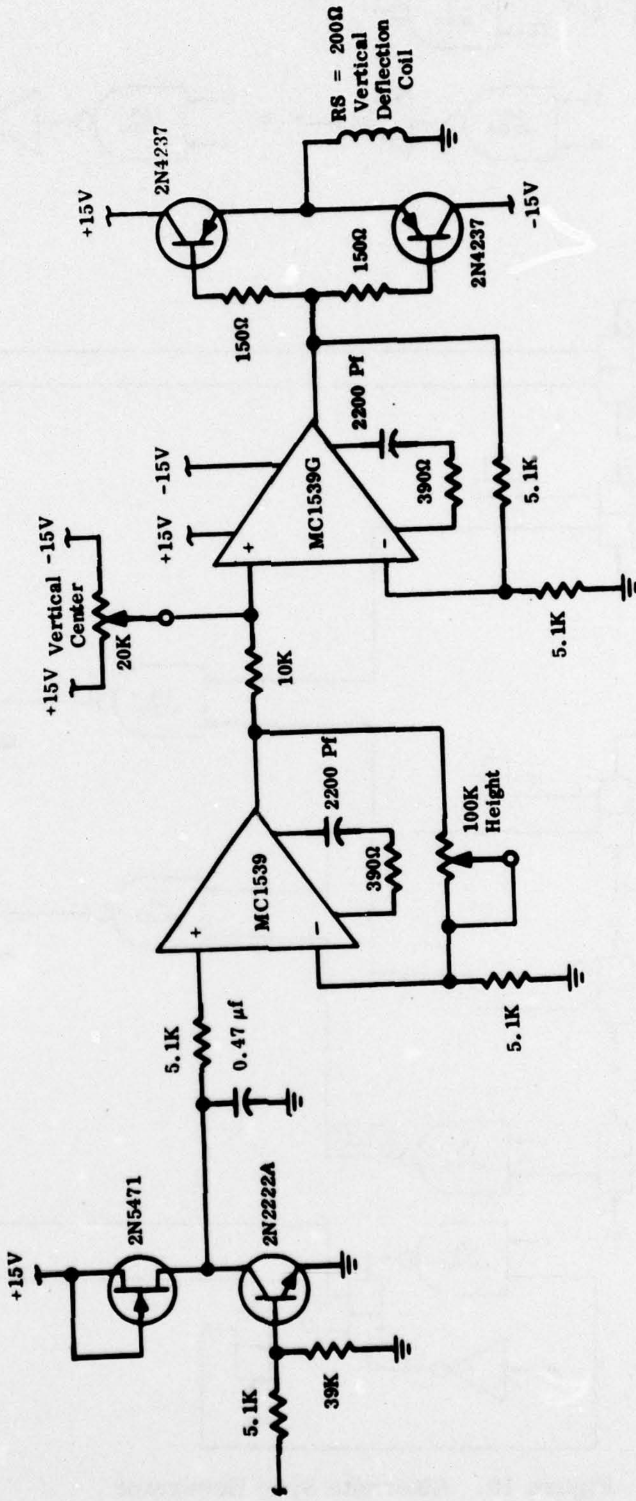


Figure 11. Vertical Deflection Alternate #1

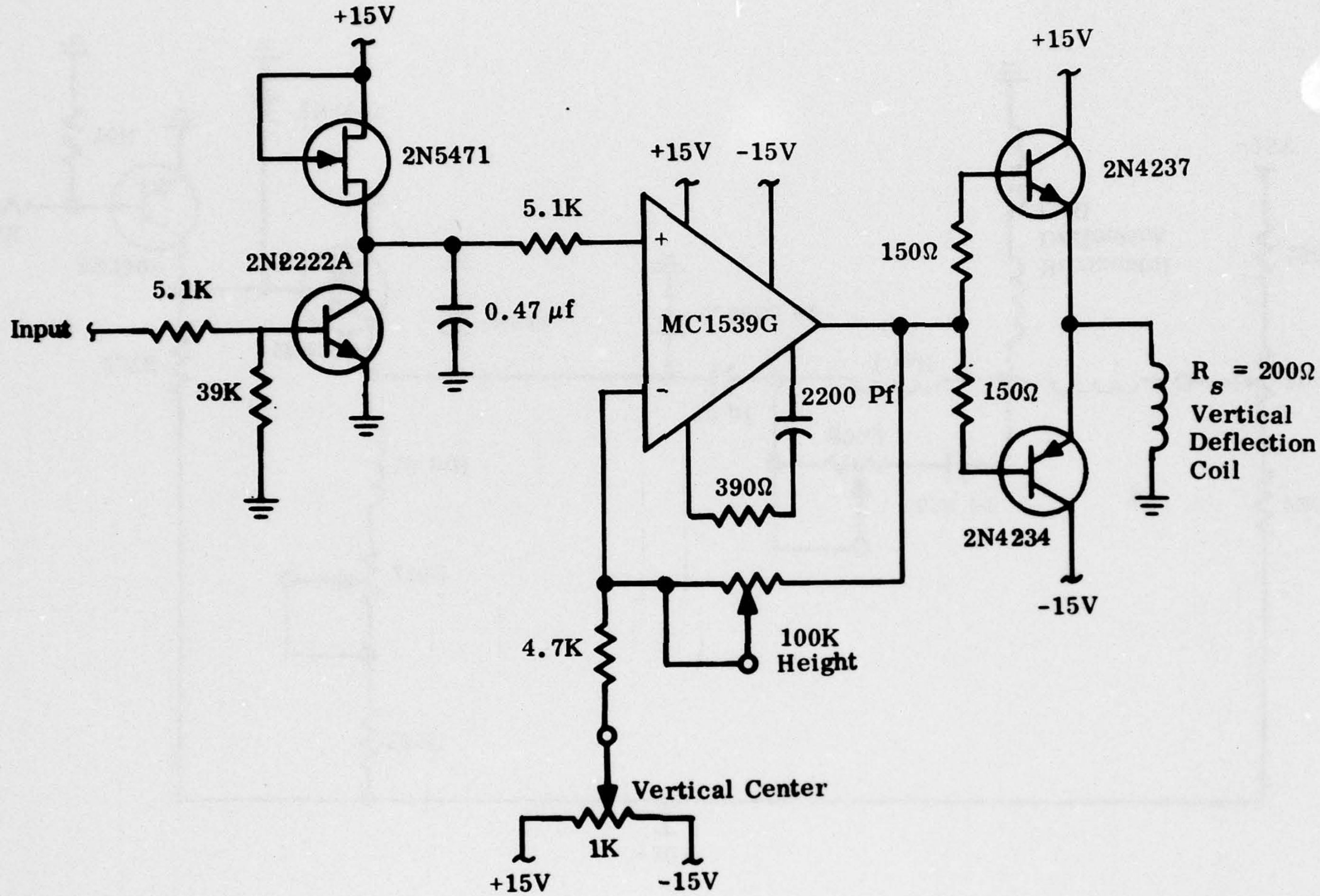


Figure 12. Vertical Deflection Circuit (Alternate #2)

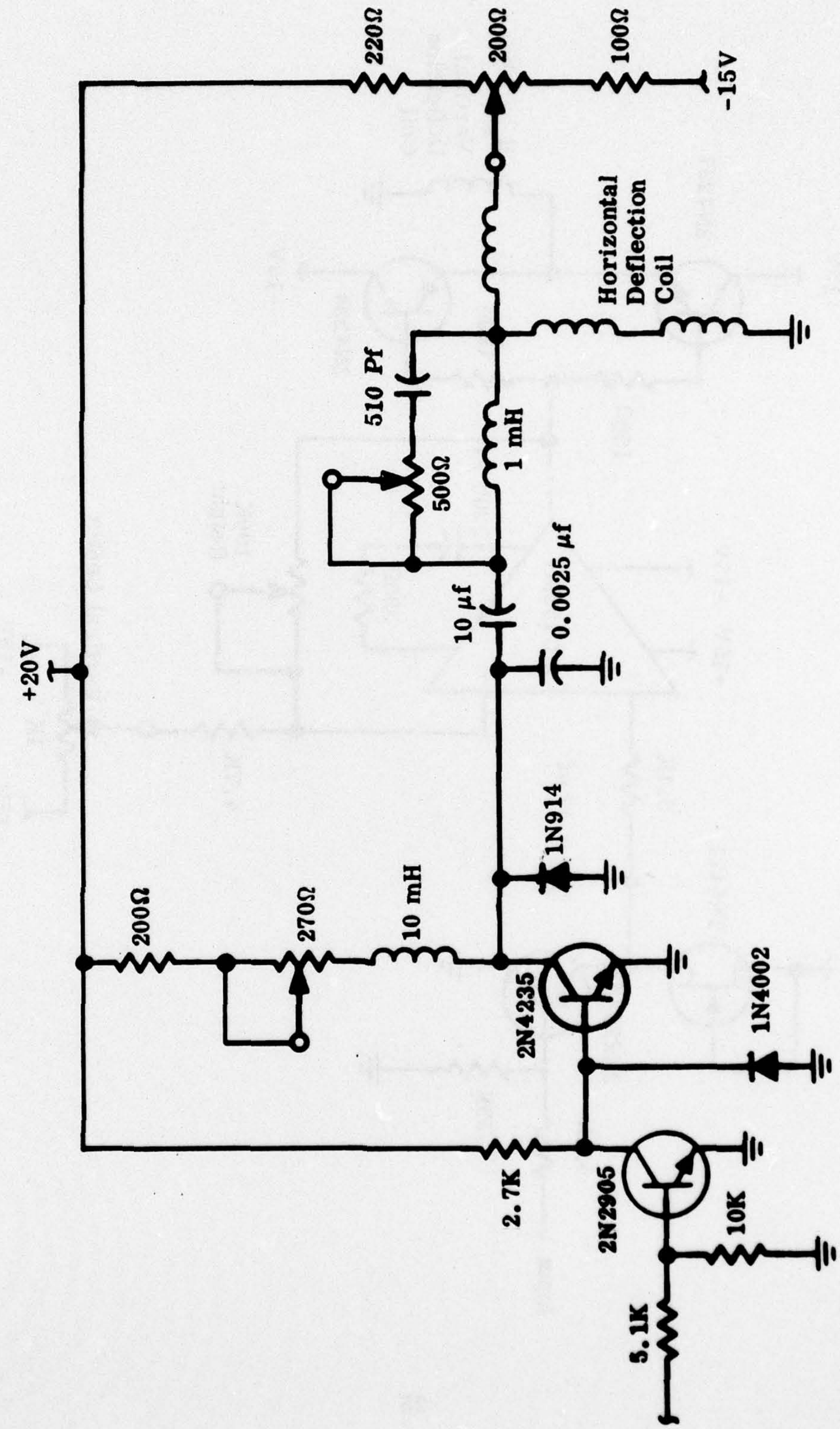


Figure 13. Horizontal Deflection

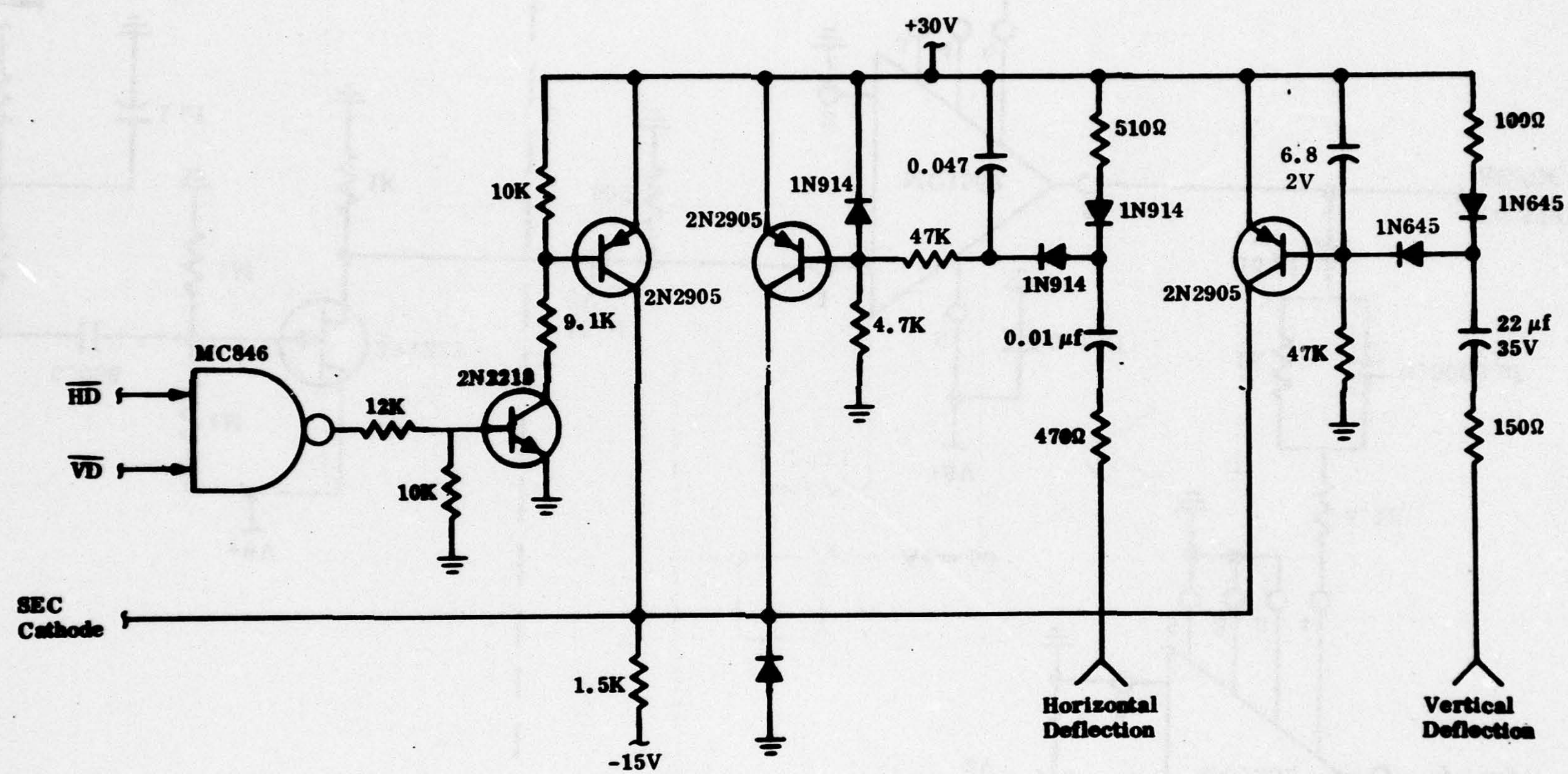
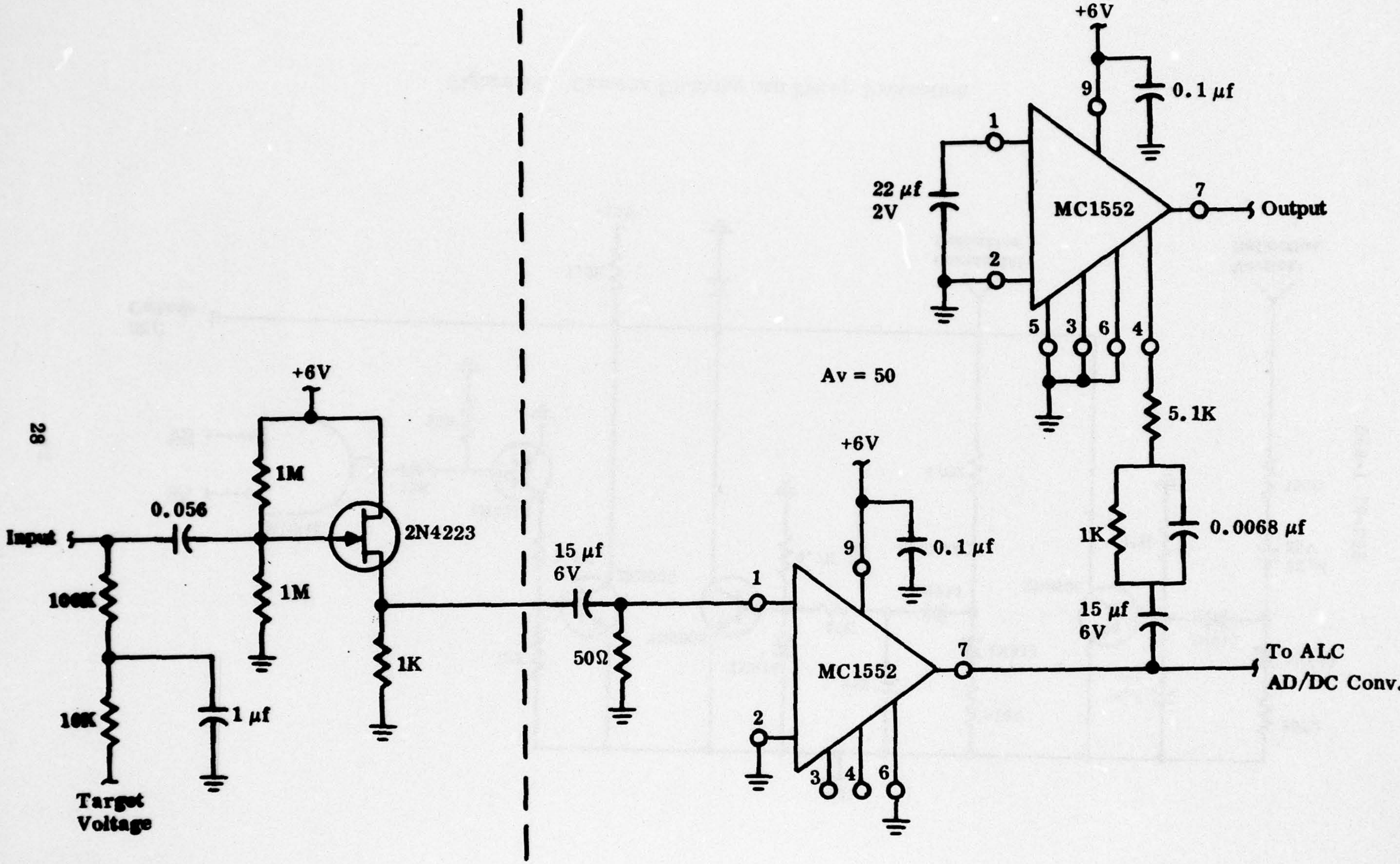


Figure 14. Camera Blanking and Sweep Protection



Video Preamplifier

Figure 15. Video Amplifier

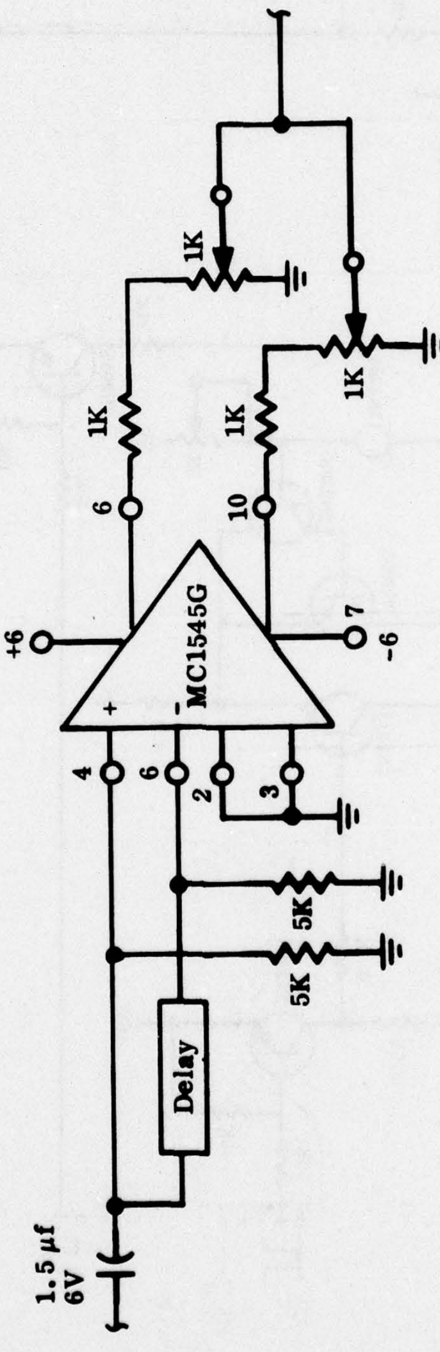


Figure 16. Aperture Correction

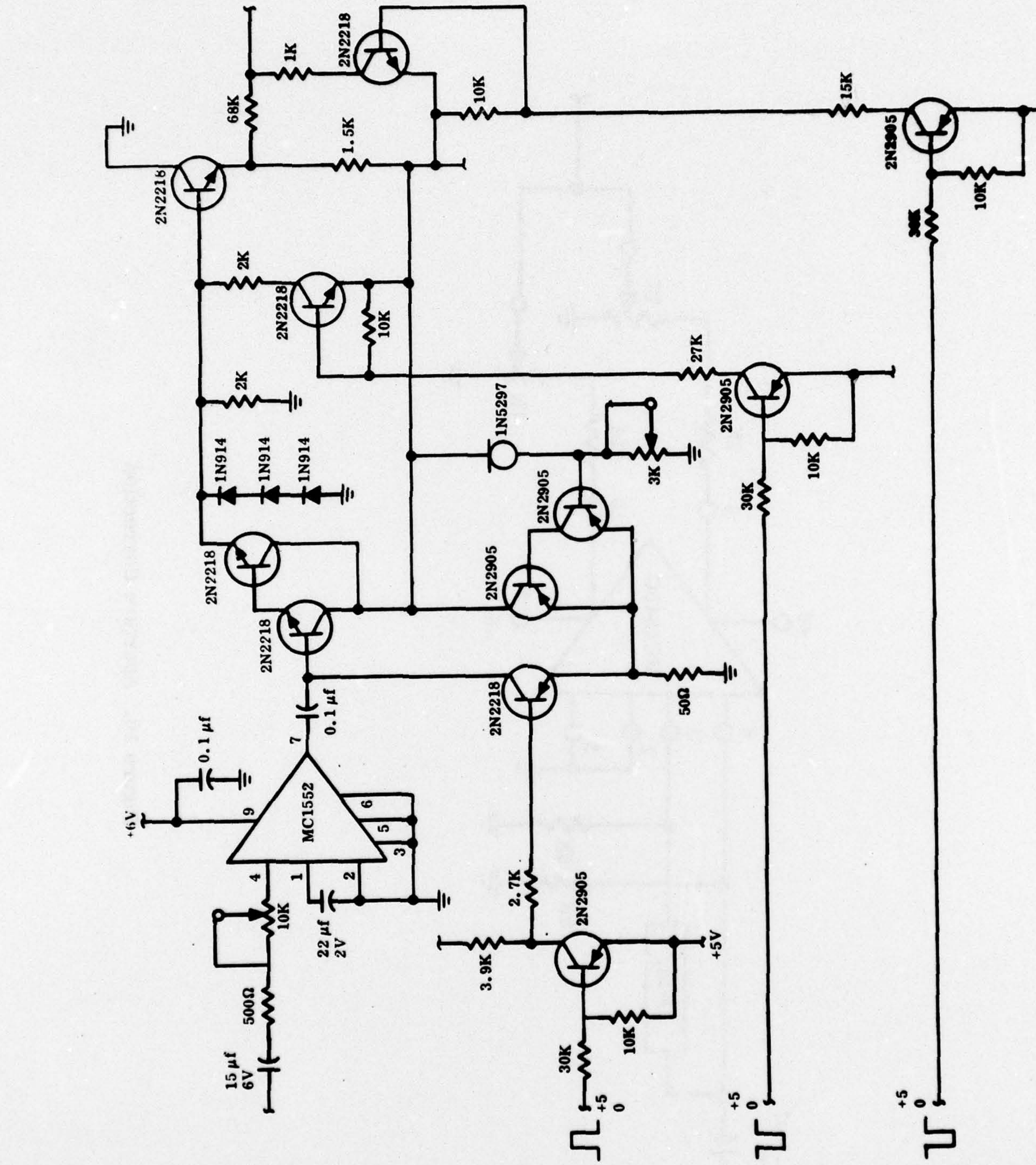


Figure 17. Video Clamp and Mixer

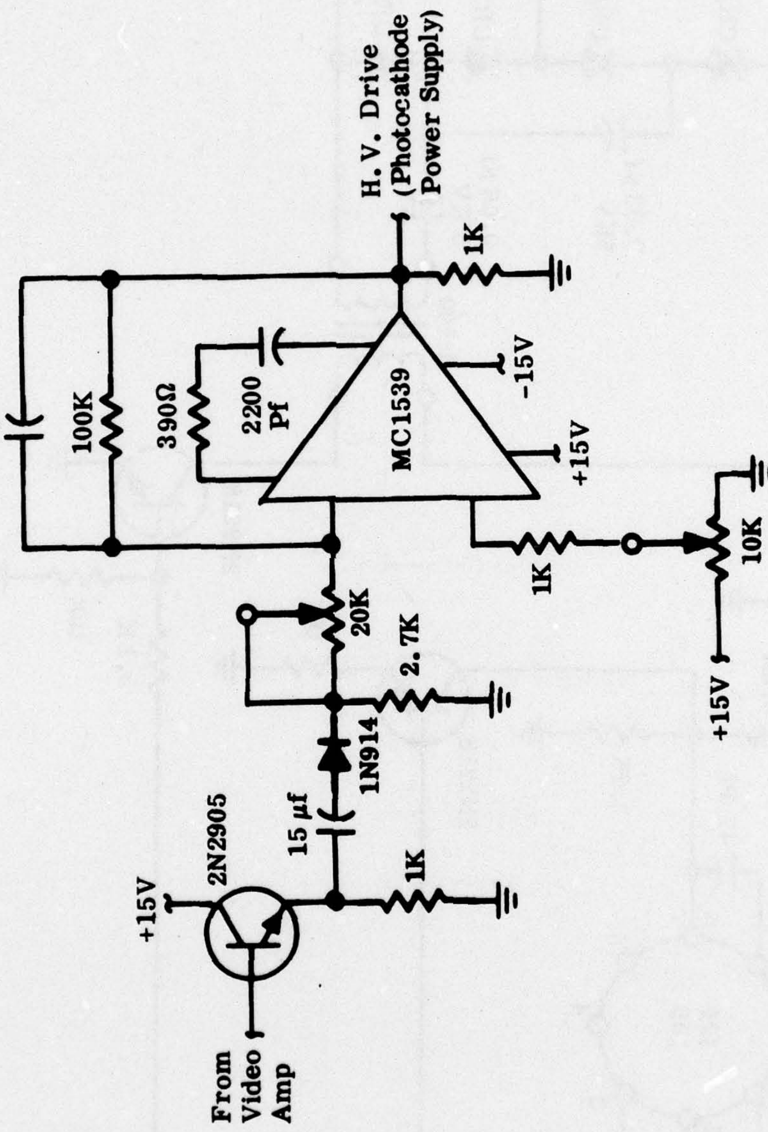
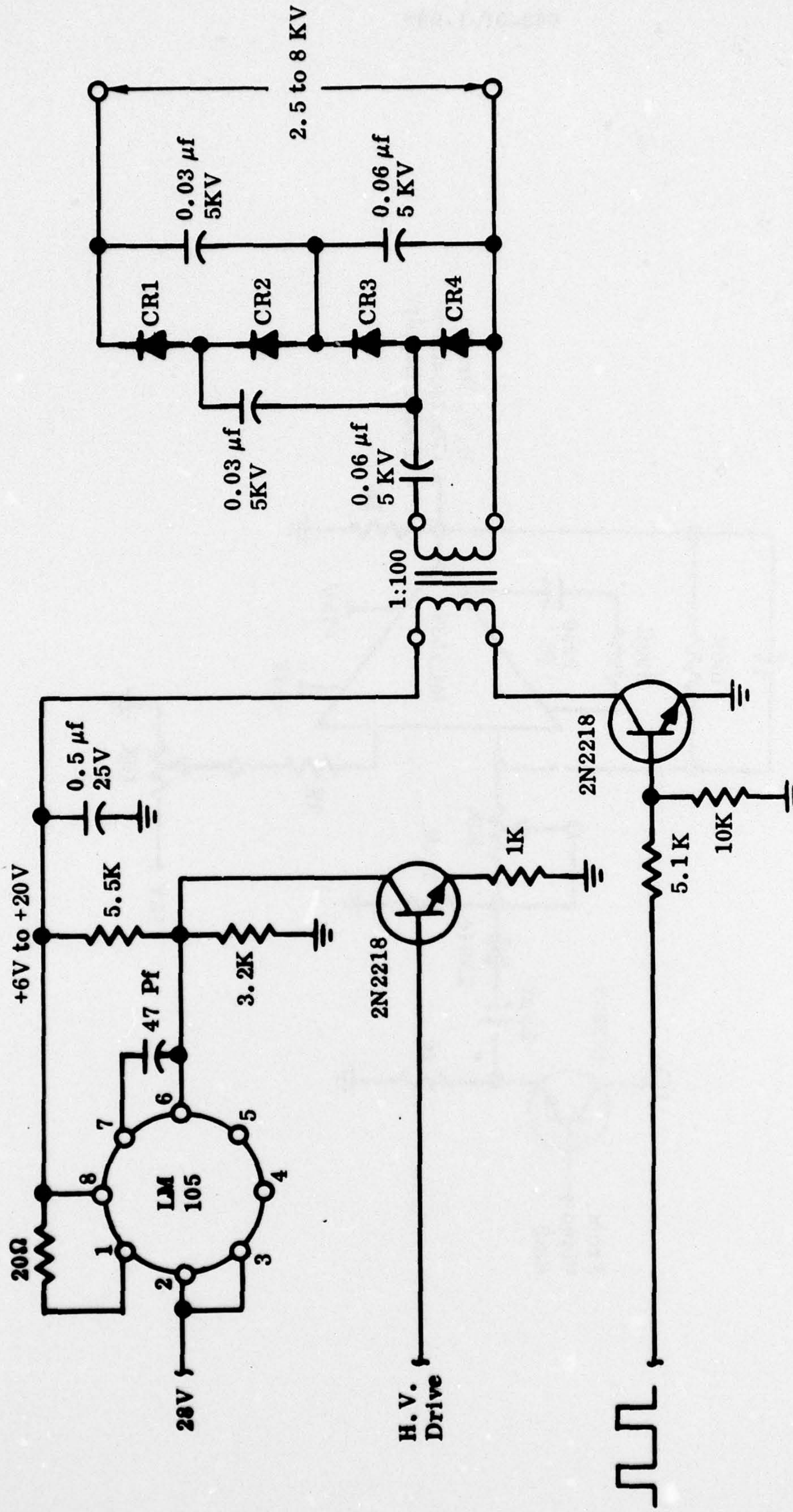


Figure 18. ALC Detector



Note: PIV of CR1-CR4 to be ≥5 KV.

Figure 19. Photocathode Power Supply

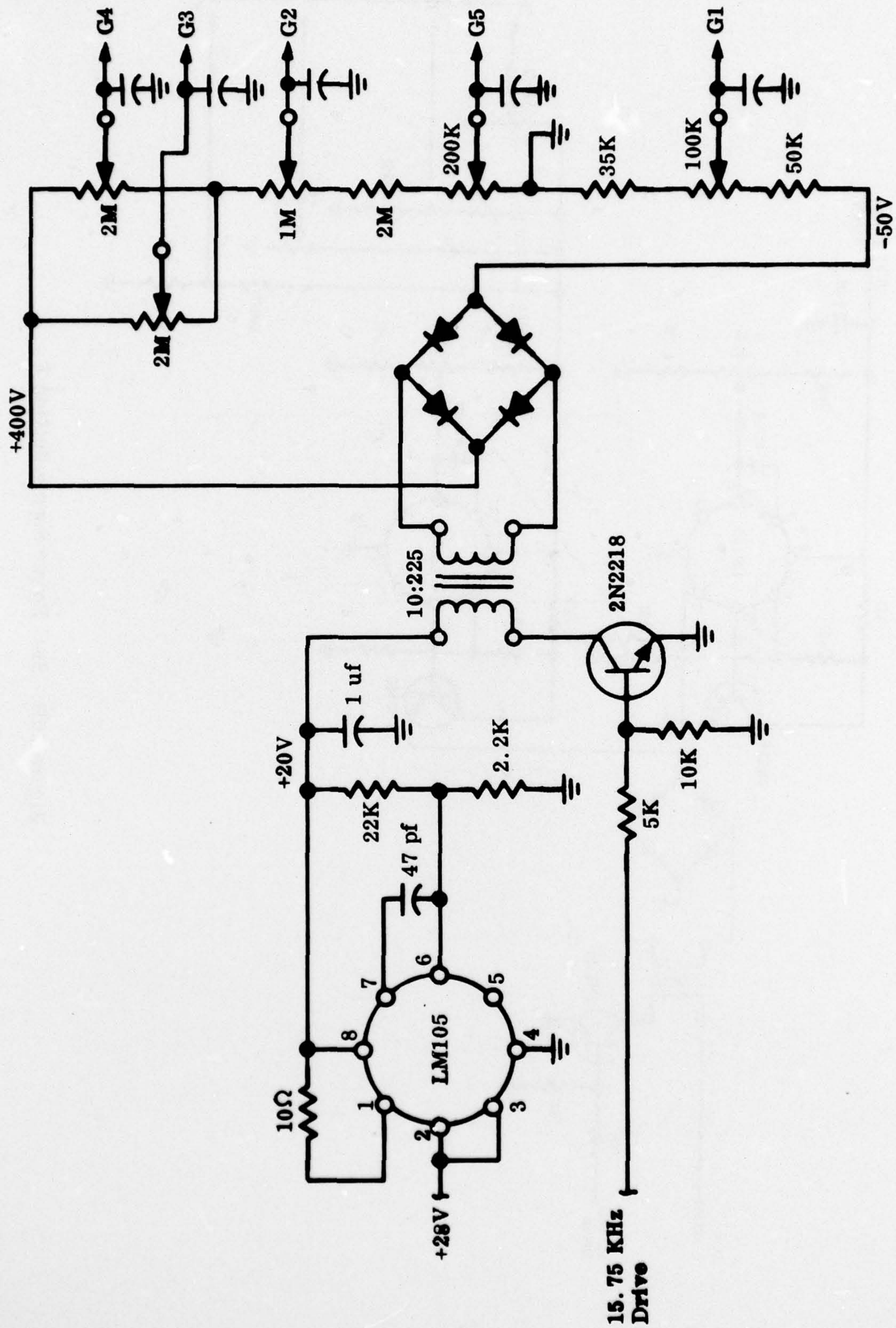


Figure 20A. SEC Power Supply, Section 1

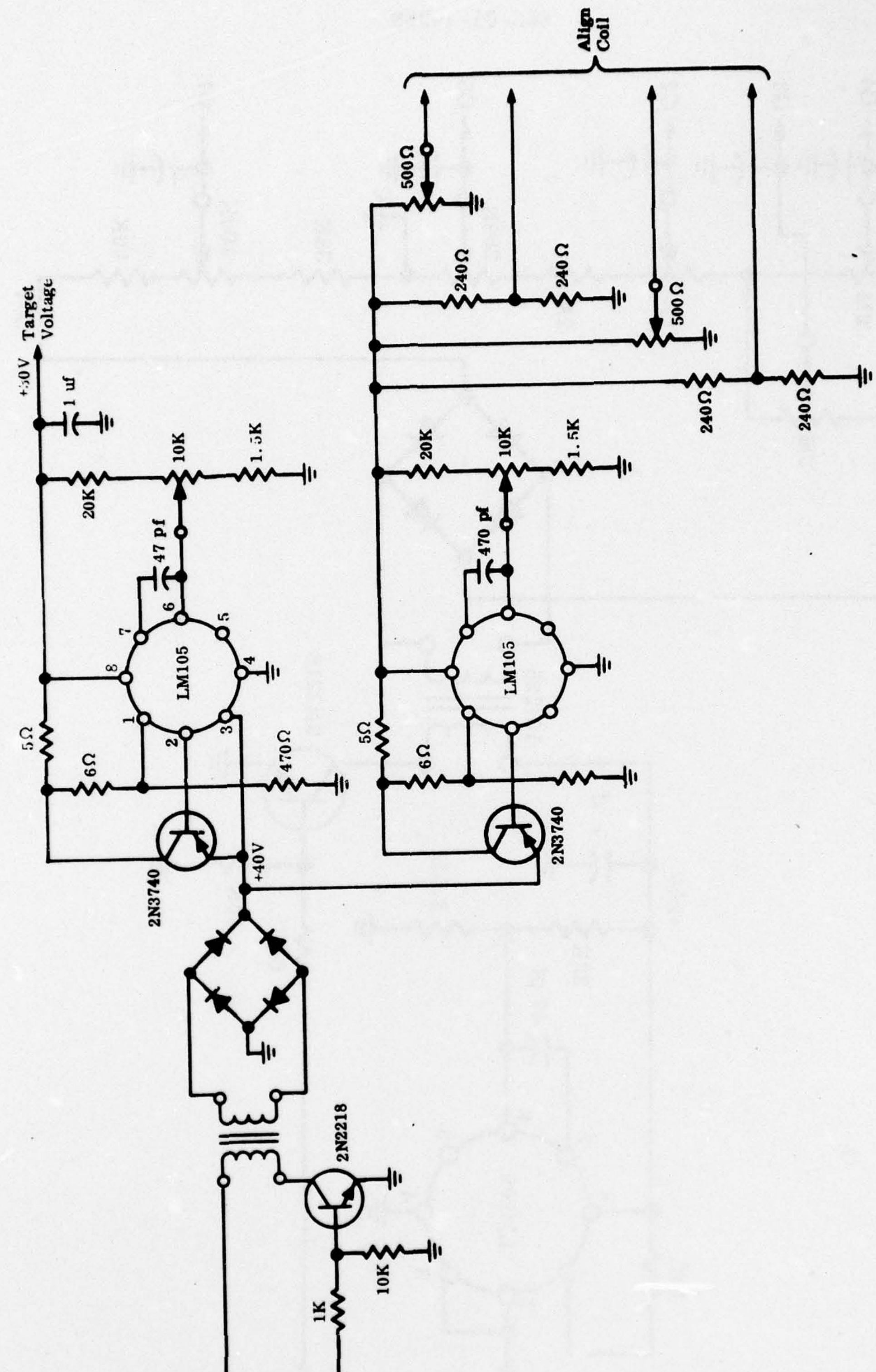


Figure 20B. SEC Power Supply, Section 2